Karunadu Technologies Private Limited
office: #17, ATK complex, 2nd and 4th Floor, Acharya College Main Road, Beside KarurVysya Bank, Guttebasaveshwaranagar, Chikkabanvara, Bengaluru, Karnataka- 560090

IEEE M.Tech, B.E, B.Tech Tittles 2020-2021
VLSI PROJECTS

Sl No	TITLE OF THE PAPER
KTVLSI001	Design and Implementation of Decoder Architecture for Non-binary LDPC Codes with Extended Min-Sum Algorithm on FPGA.
KTVLSI002	Design and Implementation of high speed, low power and high throughput Buffered and Buffer-less NoC for effective data transmission on FPGA
KTVLSI003	Design and Implementation of Elliptic Curve Cryptosystem EIGamal Encryption and Transmission Scheme on FPGA
KTVLSI004	Design and Implementation of Traffic engineered NoC for streaming applications on FPGA
KTVLSI005	Design and Implementation of Synchronous Network on Chip (NoC) for High speed and Low Power Multiprocessor Environment on FPGA
KTVLSI006	Design and Validation of Virtual Cut Through based NoC for low area and high speed data communication on FPGA
KTVLSI007	Design and Implementation of Perspective and Opportunities of Modulo 2n-1 Multipliers in Residue Number System for FIR filtering on FPGA
KTVLSI008	A Novel S-box Generation for less Arithmetic operations and high speed Cryptography System in AES
KTVLSI009	Design and Implementation of Two-Speed, Radix-4, Serial–Parallel Multiplier on FPGA
KTVLSI010	FPGA Implementation of Steller-Matrix based on Mix Column in Advance Encryption Standards.
KTVLSI011	Design and Implementation of Image and Video Processing Applications Using Xilinx System Generator on FPGA.
KTVLSI012	High-Throughput Low-Power Area-Efficient Out phasing Modulator Based on Unrolled and Pipelined Radix-2 CORDIC.
KTVLSI013	FPGA Implementation of Discrete Fourier Transform Core Using NEDA

KTVLSI014	Fetal heart beat detection by Hilbert transform and non-linear state-space projections.
KTVLSI015	New Approach to Look-up-Table Design and Memory-Based Realization of FIR Digital Filter
KTVLSI016	Analysis and Implementation of Low-cost FPGA Based Digital Pulse-width Modulator
KTVLSI017	Design and Implementations of the Hummingbird Cryptographic Algorithm on FPGA
KTVLSI018	A Fixed-Point Squaring Algorithm Using an Implicit Arbitrary Radix Number System
KTVLSI019	Design and Implementation of Logic Synthesis in Reversible PLA on FPGA
KTVLSI020	Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication
KTVLSI021	Design and Implementation of Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation on FPGA
KTVLSI022	Design and FPGA Implementation of Fused Floating-Point Four-Term Dot Product Unit
KTVLSI023	Design and Implementation of Efficient VLSI Architecture for Edge-Oriented Demosaicking on FPGA
KTVLSI024	Implementation of Memory-Based Architecture for Multicharacter Aho–Corasick String Matching on FPGA
KTVLSI025	Design and Implementation of Key-Based Dynamic Functional Obfuscation of Integrated Circuits using Sequentially-Triggered Mode-Based Design
KTVLSI026	Design and FPGA Implementation of Low-power-delay-product radix-4 8*8 Booth multiplier in CMOS
KTVLSI027	Design and Implementation of Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications
KTVLSI028	Design and Implementation of AES-128 based Secure Low Power Communication for LoRaWAN IoT Environments

KTVLSI029	Design and Implementation of High performance and energy efficient single precision and double-precision merged floating-point adder on FPGA
KTVLSI030	Design and Implementation of Low-complexity Image and Video Coding Based on an Approximate Discrete Tchebichef Transform on FPGA
KTVLSI031	Algorithm and VLSI Architecture Design of Proportionate-Type LMS Adaptive Filters for Sparse System Identification on FPGA
KTVLSI032	Design and Implantation of Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers
KTVLSI033	Design and VLSI Architecture Implementation of RC4-AccSuite: A Hardware Acceleration Suite for RC4-Like Stream Ciphers
KTVLSI034	Design and FPGA Architecture based Approximate DCT Image Compression using Inexact Computing
KTVLSI035	FPGA Implementation of Heart-Beats Based Biometric Random Binary Sequences Generation to Secure Wireless Body Sensor Networks
KTVLSI036	Design and FPGA Implementation of RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder
KTVLSI037	Design and Performance analysis of 16-order FIR filter design using different multiplication techniques on FPGA
KTVLSI038	Design and Implementation of High Throughput Implementation of SMS4 on FPGA
KTVLSI039	Design and Performance Analysis of Approximate Compressors for Multiplication on FPGA
KTVLSI040	Fully Pipelined Low-Cost and High-Quality Color Demosaicking VLSI Design for Real-Time Video Applications
KTVLSI041	Design and Implementation of Extensible FlexRay Communication Controller for FPGA-Based Automotive Systems
KTVLSI042	FPGA Based Architecture Level design of Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks
KTVLSI043	Design and FPGA Implementation of Low-complexity pipelined architecture for FBMC/OQAM transmitter
KTVLSI044	FPGA Implementation of High-speed demonstration of bit-serial floating-point adders and multipliers using single-flux-quantum circuits
KTVLSI045	Design and FPGA Implementation of Variable Latency Speculative Han-Carlson Adder
KTVLSI046	VLSI Architecture based Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block

KTVLSI047	Design and Performance analysis of High throughput and secure advanced encryption standard on field programmable gate array with fine pipelining and enhanced key expansion on FPGA
KTVLSI048	Design and Implementation of Low-Power Architecture for the Design of a One-Dimensional Median Filter on FPGA
KTVLSI049	Memory-Based Hardware Architectures to Detect ClamAV Virus Signatures with Restricted Regular Expression Features
KTVLSI050	FPGA Implementation of Fused Floating-Point Four-Term Dot Product Unit for low power and high speed
KTVLSI051	Design and FPGA Implementation of Recursive Approach to the Design of a Parallel Self-Timed Adder for low area and low power
KTVLSI052	Low power and high speed FPGA implementation of Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT
KTVLSI053	A High-Throughput and Low latency VLSI Architecture for Hard and Soft SC-FDMA MIMO Detectors on FPGA
KTVLSI054	Low power and high speed Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding and its Implementation on FPGA
KTVLSI055	Design and Implementation of Energy-Efficient Floating-Point MFCC Extraction Architecture for Speech Recognition Systems
KTVLSI056	FPGA Implementation of Low-Power Programmable PRPG With Test Compression Capabilities
KTVLSI057	FPGA implementation of Trojans through Detecting and Weakening of Cryptographic Primitives for high security
KTVLSI058	Design and Implementation of Two-Step Optimization Approach for the Design of Multiplier less Linear-Phase FIR Filters
KTVLSI059	Design and FPGA Implementation of Optimized 32-Bit Vedic Multiplier and Square Architectures
KTVLSI060	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis
KTVLSI061	Design and FPGA implementation of Novel Test-Mode-Only Scan Attack and Countermeasure for Compression-Based Scan Architectures
KTVLSI062	Design and Implementation of Discrete Tchebichef Transform Approximation for Image and Video Coding on FPGA
KTVLSI063	Design and FPGA implementation of Obfuscating DSP Circuits via High-Level Transformations
KTVLSI064	Design and FPGA implementation of An Energy Efficient Design for ECG Recording

	and R-peak Detection Based on Wavelet Transform
KTVLSI065	**FPGA Implementation of an Encryption Scheme Using Chaotic Map and Genetic Operations for Wireless Sensor Networks**
KTVLSI066	**Implementation of a New Lightweight Encryption Design for Embedded Security on FPGA**
KTVLSI067	**Design and Implementation of Key Updating for Leakage Resiliency With Application to AES Modes of Operation on FPGA**
KTVLSI068	**Design and FPGA implementation of Novel Test-Mode-Only Scan Attack and Countermeasure for Compression-Based Scan Architectures**
KTVLSI069	**Design and Implementation of Test Compression for Circuits with Multiple Scan Chains on FPGA**
KTVLSI070	**Design and FPGA Implementation of Preventing Fault Attack on Stream Cipher using Randomization**